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一种高电源抑制比的曲率补偿带隙基准电压源

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摘要：基于 0.13 μm CMOS 工艺设计了一个高阶曲率补偿带隙基准电压源，该带隙基准电压源具有低温度系数和高电源抑制比（PSRR）。通过高阶曲率补偿电路得到低温度系数；在该带隙基准电压源的核心电路中，使电流镜管的栅源电压保持恒定值来实现在一定频段下的 PSRR 增强。利用 Cadence 工具进行了仿真，并进行了流片验证，测试结果表明，该带隙基准电压源具有恒定的 1.2 V 基准电压，在 -45～165 ℃内，基准电压的温度系数为 3.95×10^{-6}/℃；PSRR 在 10 kHz下为 74.7 dB，在 1 MHz 下为 42 dB；电路启动时间为 1.4 μs。该设计已应用于高精度嵌入式电源管理芯片的低压差线性稳压器中。

关键词：带隙基准电压源；高电源抑制比（PSRR）；低温度系数；曲率补偿；启动时间
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A Curvature Compensation Bandgap Reference Voltage Source with High Power Supply Rejection Ratio

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Abstract: A high-order curvature compensation bandgap reference voltage source was designed based on 0.13 μm CMOS process with a low temperature coefficient and high power supply rejection ratio (PSRR). The low temperature coefficient was obtained by a high-order curvature compensation circuit. In the core circuit of the bandgap reference voltage source a constant gate-source voltage in the current mirror was maintained to enhance the PSRR under a certain frequency. The Cadence tool was used for the simulation, and the chip was fabricated and verified. The test results show that the bandgap reference voltage source has a constant reference voltage of 1.2 V and temperature coefficient of the reference voltage is 3.95×10^{-6}/℃ in the temperature range of -45-165 ℃. The circuit performs a PSRR of 74.7 dB@10 kHz and 42 dB@1 MHz, and the start-up time of the circuit is 1.4 μs. The design has been used in low dropout regulators in high precision implanted power management chips.

Key words: bandgap reference voltage source; high power supply rejection ratio (PSRR); low temperature coefficient; curvature compensation; start-up time
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一种带有曲率补偿的低功耗带隙基准电压源

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摘要：设计了一种带有曲率补偿的低功耗带隙基准电压源电路。该基准源电路主要由启动电路、运算放大器、正温度系数（PTAT）电路、负温度系数（CTAT）电路和曲率补偿电路组成。电路中采用 MOSFET 替代传统双极结型晶体管作为 CTAT 来源，并在一阶带隙基础上结合高阶曲率补偿技术，以降低温度系数、提高线性度。基于 CSMC 0.18 μm 工艺设计了该带隙基准电压源芯片，并将其应用于一种超低功耗的模数转换器（ADC）中。在完成 ADC 的流片后对带隙基准电压源单独进行参数测试，结果显示在 1.8 V 电源电压下，输出电压为 559 mV，在-40～130 ℃内，温度系数为 6.47×10^{-6}/℃，电源抑制比为-54.26 dB，总工作电流仅为 0.48 μA，芯片面积为0.003 7 mm^2。

关键词：带隙基准；低功耗；曲率补偿；温度系数；模数转换器（ADC）
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A Low Power Consumption Bandgap Reference Voltage Source with Curvature Compensation

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Abstract: A low power consumption bandgap reference voltage source circuit with curvature compensation was designed. The reference source circuit was mainly composed of the starting circuit, operational amplifier, proportional to absolute temperature (PTAT) circuit, complementary to absolute temperature (CTAT) circuit and curvature compensation circuit. In the circuit, MOSFETs were used to replace conventional bipolar junction transistors as the CTAT source, and the high-order curvature compensation technology was applied additionally on the basis of the first-order bandgap to reduce the temperature coefficient and improve the linearity. The chip was designed based on CSMC 0.18 μm process and applied in an ultra-low power consumption analog-to-digital converter (ADC). Parameter testing for the bandgap reference source was performed after the ADC was fabricated. The results show that the output voltage is 559 mV at a power supply voltage of 1.8 V. The temperature coefficient is 6.47×10^{-6}/℃ in a temperature range of -40-130 ℃. The power supply rejection ratio is -54.26 dB. The total operating current is only 0.48 μA, and the chip area is 0.003 7 mm^2.

Key words: bandgap reference; low power consumption; curvature compensation; temperature coefficient; analog-to-digital converter (ADC)
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一款低相位噪声的可编程分频器

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摘要：设计了一款低相位噪声的可编程分频器，主要用于高鉴相频率的锁相环频率源中。电路设计采用2/3分频器级联结构，通过数选电路实现连续可变分频。从相位噪声产生机理、噪声来源及相位噪声与抖动的关系等方面分析影响分频器相位噪声的关键因素，通过工艺选择、电路设计和仿真分析来优化分频器的相位噪声。采用0.13 μm SiGe BiCOMS工艺进行了设计仿真和流片，芯片面积为1.3 mm^2。测试结果表明：该分频器最高工作频率为20 GHz，电源电压为+3.3 V，最大电流为80 mA，可实现1~31连续分频，在输入6 GHz正弦波信号下20分频时的相位噪声为-145 dBc/Hz@1 kHz。

关键词：低相位噪声；分频器；锁相环（PLL）；SiGe；BiCOMS工艺
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A Programmable Frequency Divider with Low Phase Noise

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Abstract: A programmable frequency divider with low phase noise was designed, which is mainly used in phase-locked loop (PLL) frequency source with high phase detection frequency. A 2/3 frequency divider cascaded structure was adopted in the circuit of the programmable frequency divider. The continuous variable frequency division was realized through digital selective circuit. The key factors affecting the phase noise of the frequency divider were analyzed in terms of the generation mechanism of the phase noise, the noise source and the relationship between the phase noise and jitter. The phase noise of the frequency divider was optimized by the process selection, circuit design, and simulation analysis. The frequency divider chip with an area of 1.3 mm^2 was designed and fabricated using the 0.13 μm SiGe BiCOMS process. The test results show that the maximum operating frequency is 20 GHz, the power supply voltage is +3.3 V, and the maximum current is 80 mA. The frequency divider can achieve 1~31 continuous frequency division. The phase noise of the 6 GHz input sinusoidal signal is -145 dBc/Hz@1 kHz at 20-frequency division.

Key words: low phase noise; frequency divider; phase-locked loop (PLL); SiGe; BiCOMS process

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用于车载以太网物理层芯片的降压电路

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摘要：为了给车载以太网物理层芯片内部的数字电路提供稳定的电源，设计了一种 3.3 V 转换到 1.2 V±25 mV 的 DC-DC 降压（Buck）电路。电路采用恒定导通时间控制模式，包括片内集成的软启动电路、定时器、过零检测电路和死区时间控制电路。该 Buck 电路基于 SMIC 0.13 μm CMOS 工艺实现，并已集成到物理层芯片内部。测试结果表明，电路能够实现 3.3 V 转换到 1.2 V±25 mV 的功能；带载电流为 100.9 mA，转换效率达到 91%；定时器产生的恒定导通时间为 410 ns；启动过程中输出电压变化较为平稳，没有过冲，最后稳定在 1.194 V±25.25 mV，启动时间为 250 μs。

关键词：物理层；开关稳压器；降压（Buck）电路；恒定导通时间控制；软启动电路
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Buck Circuit for the Automotive Ethernet Physical Layer Chip

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Abstract: In order to provide a stable power supply for digital circuits inside automotive Ethernet physical layer chips, a DC-DC Buck circuit which converts a voltage from 3.3 V to 1.2 V±25 mV was designed. The constant on-time control mode was adopted. The circuit includs the on-chip integrated soft-startup circuit, timer, zero-crossing detection circuit and dead-time control circuit. The Buck circuit was realized based on the SMIC 0.13 μm CMOS process and was integrated into the physical layer chip. The test results show that the circuit can achieve the function of the voltage conversion from 3.3 V to 1.2 V±25 mV, the load current is 100.9 mA, the conversion efficiency reaches 91%, and the constant on-time generated by the timer is 410 ns. The output voltage changes smoothly without overshoot during the startup process and finally stabilizes at 1.194 V±25.25 mV and the startup time is 250 μs.

Key words: physical layer; switching regulator; Buck circuit; constant on-time control; soft-startup circuit

EEACC: 1210

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Ⅲ-Ⅴ/Si 混合集成波导高效耦合的容差范围

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摘要：Ⅲ-Ⅴ/Si 混合集成的反馈外腔半导体光源及其相关集成器件成为近年来的研究热点，大容差范围是该类器件提高成品率和降低制备成本的有效途径。采用有限差分光束传播法，针对应用于大尺寸Ⅲ-Ⅴ/Si 混合集成波导的双锥形耦合器结构进行了仿真，研究了实现高效耦合结构参数容差范围。结果表明，当Ⅲ-Ⅴ材料有源波导中缓冲层厚度为 0.5~0.7 μm，有源波导锥形区长度为 400~800 μm，锥形区尖部宽度为 0.5~0.55 μm，有源波导增益区宽度为 2.9~3.1 μm，无源波导锥形区的长度超过 500 μm，有源波导相对于 Si 波导的偏移量小于 1 μm 时，Ⅲ-Ⅴ/Si 混合集成波导的耦合效率均可达到 90%以上。研究双锥形Ⅲ-Ⅴ/Si 波导高效耦合参数的容差范围可为下一步制备出高效耦合的该类大尺寸混合集成器件提供参考。

关键词：Ⅲ-Ⅴ/Si 混合集成波导；耦合效率；双锥形耦合器；有限差分光束传播法（FD-BPM）；容差范围

中图分类号：TN256；TN304.12　文献标识码：A　文章编号：1003-353X（2019）12-0925-07

Tolerance Range of the Ⅲ-Ⅴ/Si Hybrid Integrated Waveguide for High Efficiency Coupling

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Abstract: Ⅲ-Ⅴ/Si hybrid integrated feedback external cavity semiconductor light source and related integrated devices have become research hotspots in recent years. The large tolerance range is an effective way to improve the yield and reduce the manufacturing cost of the devices. The finite-difference beam propagation method was used to simulate the dual taper coupler structure applied to the large-size Ⅲ-Ⅴ/Si hybrid integrated waveguide, and the tolerance range of the high-efficiency coupling structure parameter was studied. The results show that the coupling efficiency of the Ⅲ-Ⅴ/Si hybrid integrated waveguide can be achieved at least 90% when the thickness of the buffer layer in the Ⅲ-Ⅴ materials active waveguide is 0.5-0.7 μm, the length of the active waveguide cone is 400-800 μm, the width of the tapered tip is 0.5-0.55 μm, the width of the waveguide gain region is 2.9-3.1 μm, the length of the tapered portion of the passive waveguide exceeds 500 μm, and the offset of the active waveguide relative

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环栅纳米线 FET 自热效应及微尺度空间效应研究

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摘要：研究了纳米线高度与纳米线宽度对 5 nm 制程垂直堆叠式环栅纳米线场效应晶体管（GAA NWFET）中自热效应及微尺度空间效应的影响机理。利用 Sentaurus TCAD 软件对不同尺寸的纳米线器件性能进行仿真，采用控制变量法，以 0.5 nm 为步长，分别将纳米线高度及宽度从4 nm增加至 8 nm。仿真结果表明，当纳米线高度及宽度分别取 4 nm 和 6.5 nm 时，可最大程度规避微尺度空间效应对载流子迁移率的影响，并有效提升散热能力，使器件开态电流增加44.4%，沟道热学电阻减小 60.3%。此外，设置纳米线高度为 4 nm，依次将顶部/中部/底部沟道的纳米线宽度从 6.5 nm 增加至 8 nm，发现当底部沟道的纳米线宽度相等时，增加靠近体硅处的沟道宽度更有利于改善器件的电热性能。

关键词：环栅；垂直堆叠结构；自热效应；微尺度空间效应；纳米线
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Investigation of Self-Heating Effect and Microscale Spatial Effect for Gate-All-Around Nanowire FET

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Abstract: The effect mechanism of height and width of nanowires on the self-heating effect and microscale spatial effect of the vertically stacked gate-all-around nanowire field effect transistor (GAA NWFET) in 5 nm technology were investigated. The performances of different sizes of nanowire devices were simulated by Sentaurus TCAD software. Using the control variable method, the height and width of the nanowires were increased from 4 nm to 8 nm in steps of 0.5 nm, respectively. The simulation results show that when the height and width of the nanowires are 4 nm and 6.5 nm, respectively, the influence of the micro-scale spatial effect on the carrier mobility can be largely avoided, and the heat dissipation capability is effectively improved. The on-state current of the device increases 44.4% and the channel thermal resistance decreases 60.3%. In addition, when the height of the nanowire is 4 nm, the width of the nanowires of the top/middle/bottom channel is sequentially increased from 6.5 nm to 8 nm. And it is found that when the width of the nanowires of the bottom channel is equal, the increase of the channel width close to the bulk silicon is more conducive to improve the electrothermal performance of the device.

Key words: gate-all-around; vertically stacked structure; self-heating effect; microscale spatial effects; nanowire

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130 nm CMOS 工艺中应力对 MOS 器件饱和电流的影响

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摘要：在深亚微米 CMOS 集成电路制造工艺中，应力对 MOS 器件性能的影响已经不可忽略。应力可以改变半导体载流子的迁移率，因此影响 MOS 器件的饱和电流。通过对不同版图布局的 MOS 器件饱和电流进行分析，研究了 130 nm CMOS 工艺中浅槽隔离（STI）和金属硅化物引起的应力对器件饱和电流的影响。结果表明，器件沟道长度方向的 STI 应力使 PMOS 器件饱和电流提高 10%左右，同时使 NMOS 器件饱和电流降低 20%～30%；而沟道宽度方向 STI 应力使 NMOS 器件饱和电流降低 16%～20%，使 PMOS 器件饱和电流降低 14%。相对来说，除了沟道长度方向的金属硅化物拉伸应力对 NMOS 器件影响较大外，金属硅化物引起的其他应力对 MOS 器件性能的影响较弱。通过对 130 nm CMOS 工艺应力的分析，可以指导版图设计，从而改善器件和电路性能。

关键词：浅槽隔离（STI）；金属硅化物；饱和电流；应力；版图设计
中图分类号：TN386.1　文献标识码：A　文章编号：1003-353X（2019）12-0938-07

Effect of Stress on the Saturation Current of MOS Devices in 130 nm CMOS Process

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Abstract: In the deep submicron CMOS integrated circuit manufacturing technology, the effect of stress on performance of MOS devices cannot be ignored. Stresses change the mobility of semiconductor carriers and affect the saturation current of MOS devices. Based on the analysis of the saturation current of MOS devices with different layouts, the influence of the stress induced by shallow trench isolation (STI) and silicide on the saturation current of MOS devices in 130 nm CMOS process was studied. The results show that STI stress in the channel length direction increases the saturation current of PMOS devices by about 10%, meanwhile, it reduces the saturation current of NMOS devices by 20%～30%. STI stress in channel width direction reduces the saturation currents of NMOS devices and PMOS devices by 16%～20% and 14%, respectively. Relatively, except the obvious impact on NMOS device performance from the silicide-induced tensile stress along the channel length direction, other stresses induced by silicide has a weak influence on the performance of MOS devices. Through the analysis of the stress in 130 nm CMOS process, the device layout design can be guided and the device and circuit performance can be improved.

Key words: shallow trench isolation (STI); silicide; saturation current; stress; layout design
EEACC: 2560

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覆盖银纳米线层硅基 MEMS 过滤芯片

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摘要：通过在悬栅状微结构支架上涂覆银纳米线，制备出亚微米级孔径的微电子机械系统（MEMS）过滤芯片，并研究了该芯片的颗粒过滤性能以及相关影响因素。利用感应耦合等离子体（ICP）深硅刻蚀工艺，在二氧化硅片上双面刻蚀形成悬栅状结构。随后，利用分散液中银纳米线的均匀分布性和高比表面积，将高长径比的银纳米线均匀地涂覆到此结构的亲水性二氧化硅层上。干燥后，在重力及液体挥发作用下银纳米线和支架层紧密贴合，制成覆盖银纳米线过滤层的硅基 MEMS 过滤芯片。与硅基支架结构相比，覆盖较低质量浓度银纳米线的芯片对 $PM_{10-2.5}$的过滤效率提高了 2.5 倍，达到 73.79%，压差仅增加了 30 Pa（空气流速为 0.33 m/s）。当芯片覆盖有较高质量浓度的银纳米线时，$PM_{2.5}$ 过滤效率达到 86.63%；$PM_{10-2.5}$ 过滤效率上升到 96.67%。在相同测试条件下，过滤芯片压差增加到 1 200 Pa。

关键词：微电子机械系统（MEMS）；二氧化硅；感应耦合等离子体（ICP）刻蚀；颗粒过滤；银纳米线

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Silicon-Based MEMS Filter Chip Coated with Silver Nanowire Layer

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Abstract: A micro-electromechanical system (MEMS) filter chip with sub-micron diameter of aperture was fabricated by coating silver nanowires on the suspended grid micro-structure frame. The particle filtration performance of the filter chip and related impact factors were studied. Using the inductively coupled plasma (ICP) deep silicon etching process, a double-sided etching on a SiO_2 wafer formed the suspended grid structure. Subsequently, the high aspect ratio silver nanowires were uniformly coated on the hydrophilic SiO_2 layer of the structure using the uniform distribution and high specific surface area of the silver nanowires in the dispersion. After drying, the silver nanowires and frame layer were laminated tightly under the action of gravity and liquid evaporation. The silicon-based MEMS filter chip with a silver nanowire filter layer was prepared. Compared with the silicon-based frame structure, the $PM_{10-2.5}$ filtration efficiency of the chip covering lower mass concentration of silver nanowires increases by 2.5 times to

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用于 C 波段的薄膜体声波谐振器滤波器

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摘要：研制了一种工作于 C 波段的薄膜体声波谐振器（FBAR）滤波器。首先利用 FBAR 的一维 Mason 等效电路模型对谐振器进行设计，然后采用实际制作的谐振器模型构成阶梯型结构 FBAR 滤波器，利用 ADS 软件对 FBAR 滤波器进行电路原理图以及版图设计优化。仿真结果表明，滤波器的中心频率为 5.5 GHz，中心插损为 1.79 dB，1 dB 带宽为 115 MHz，5.3 GHz 处抑制为 40.29 dBc，5.7 GHz 处抑制为 64.32 dBc。采用空气隙结构实现了 C 波段 FBAR 滤波器芯片，并采用陶瓷外壳进行气密封装。测试结果显示，滤波器的中心插损为 2.19 dB，1 dB 带宽为 111 MHz，5.3 GHz 处抑制为 26.88 dBc，5.7 GHz 处抑制为 60.96 dBc。对测试结果与仿真结果的差异进行了分析。

关键词：薄膜体声波谐振器（FBAR）；滤波器；C 波段；一维 Mason 模型；空气隙；芯片
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A Film Bulk Acoustic Resonator Filter for C Band Application

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Abstract: A kind of film bulk acoustic resonator (FBAR) filter for C band application was developed. The resonator was designed using one dimensional Mason equivalent circuit model firstly. On the basis of the prepared resonator model, the ladder FBAR filter was established. The circuit schematic and layout of the FBAR filter was designed and optimized by ADS software. The simulation results show that the filter center frequency is 5.5 GHz, the insertion loss at center frequency is 1.79 dB, the 1 dB bandwidth is 115 MHz, and the rejections at 5.3 GHz and 5.7 GHz are 40.29 dBc and 64.32 dBc, respectively. The FBAR filter chip was realized using air-gap structure. The ceramic package was used in order to ensure hermetization. The measured results show that the filter insertion loss at center frequency is 2.19 dB, the 1 dB bandwidth is 111 MHz, and the rejections at 5.3 GHz and 5.7 GHz are 26.88 dBc and 60.96 dBc, respectively. The differences between measured results and simulation results were analyzed.

Key words: film bulk acoustic resonator (FBAR); filter; C band; one dimensional Mason model; air gap; chip

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半导体材料
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用于辐射探测器的低 Fe 掺杂半绝缘 InP 材料

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摘要：基于半绝缘 InP 衬底的辐射探测器在 X 射线成像领域有着广阔的应用前景。半绝缘 InP 衬底中 Fe 的掺杂量对 InP 基辐射探测器的性能有一定的影响。通过液封直拉（LEC）法和垂直梯度凝固（VGF）法生长了掺 Fe 半绝缘 InP 单晶，并对普通 Fe 掺杂（0. 3 g/kg）和低 Fe 掺杂的 InP 单晶的电参数特性、光学特性及辐射特性等方面进行了研究。测试数据表明 VGF 生长的 InP 单晶的位错密度小于 500 cm^{-2}，缺陷非常少。但 VGF 必须使用多晶 InP 作为原料，Fe 的掺杂量不能低于 0. 3 g/kg，造成晶体中的杂质含量较高。低 Fe 掺杂 LEC 生长的 InP 单晶的掺杂量只有普通掺杂的一半，经过退火，低 Fe 掺杂 LEC 生长的 InP 的电阻率达到 4.9×10^{7} Ω · cm，迁移率达到 4 410 $cm^{2} \cdot V^{-1} \cdot s^{-1}$，位错密度小于 1×10^{4} cm^{-2}，显示出了较好的半绝缘特性且晶体质量良好。使用低 Fe 掺杂半绝缘 InP 制成的辐射探测器显示出了良好的性能。

关键词：磷化铟（InP）；晶体生长；Fe 掺杂；半绝缘；辐射探测器
中图分类号：TN304. 23　　文献标识码：A　　文章编号：1003-353X（2019）12-0956-05

Low Fe-Doped Semi-Insulating InP Material for Radiation Detector

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Abstract: The radiation detector based on semi-insulating InP substrate has a broad application prospect in the field of X-ray imaging. The doping amount of Fe in semi-insulating InP substrate has a certain influence on the performance of InP-based radiation detector. Fe-doped semi-insulating InP single crystals were grown by liquid encapsulated Czochralski (LEC) and vertical gradient freeze (VGF) methods. The electrical parameters, optical and radiation properties of normal Fe-doped (0. 3 g/kg) and low Fe-doped InP single crystals were studied. The test data show that the VGF-grown InP single crystal has a dislocation density of less than 500 cm^{-2} and very few defects. However, the poly-InP must be used as a raw material for VGF, and the doping amount of Fe should not be less than 0. 3 g/kg, which results in high impurity content in the crystal. The doping amount of the low Fe-doped LEC-grown InP single crystal is only half of that of the normal doping. After annealing, the resistivity of low Fe-doped LEC-grown InP reaches 4.9×10^{7} Ω · cm, the mobility reaches 4 410 $cm^{2} \cdot V^{-1} \cdot s^{-1}$, and the dislocation density is less than 1×10^{4} cm^{-2}, which shows good semi-insulating property and good crystal quality. The radiation detector made of low Fe-doped semi-insulating InP shows good performance.

Key words: InP; crystal growth; Fe doping; semi-insulating; radiation detector

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一种锂离子电池管理芯片的失效定位

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摘要：针对一种锂离子电池管理芯片的失效定位进行了研究。某单机在测试时由于锂离子电池管理芯片失效，导致所采集的电压数据间歇异常跳变。经一致性分析，发现失效锂离子电池管理芯片老炼后的转换功耗和回读功耗与同批次芯片相比异常增加。通过微光分析和版图对比，发现失效芯片中菊花链电流比较器的 NMOS 管存在漏电缺陷。对比较器工作原理进行进一步分析，并分析了 SCLK 接口和 CNVST 接口的翻转阈值与功耗变化量之间的关系，确认了芯片失效是由于 NMOS 管漏电所导致，且通过电老炼可以暴露 NMOS 管的漏电缺陷。最后，针对器件功耗变化量与内部 NMOS 管漏电之间的关系进行了仿真和计算，定量验证了锂离子电池管理芯片老炼后功耗的增加是由于比较器 NMOS 管漏电引起的。

关键词：锂离子电池管理芯片；失效；比较器；功耗；翻转阈值
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Failure Localization of a Lithium-Ion Battery Management Chip

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Abstract: The failure localization of a lithium-ion battery management chip was studied. The acquired voltage data of a single-machine intermittently jumped during testing caused by the failure of a lithium-ion battery management chip. After consistency analysis, it is found that the conversion power consumption and the read-back power consumption of the failure chip are abnormally higher than those of the same batch chips. Through emission microscopy and layout comparison, it is found that the NMOSFET in the daisy chain current comparator of the failure chip has a leakage failure. The operational principle of the comparator was further analyzed, and the relationship between the reversal threshold and the power consumption variation of the SCLK and CNVST interfaces were analyzed. It is confirmed that the chip failure is cause by the leakage of the NMOSFET, and the leakage failure can be exposed through an burn-in test. The correlation between the power consumption variation of the chip and the leakage of the internal NMOSFET were simulated and calculated. It is quantitatively verified that the increase of the power consumption of the lithium-ion battery management chip after the burn-in test is caused by the leakage of the

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基于 FRD 芯片准 TCP 电流的 IGBT 模块老化在线监测方法

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摘要：在变流器超同步等工况下，绝缘栅双极晶体管（IGBT）模块中的快恢复二极管（FRD）相比于 IGBT 更容易老化，因此，对 IGBT 模块中 FRD 状态的在线监测至关重要。通过理论与实验研究了 FRD 正向特性曲线的温度依赖性，并定义了准温度补偿点（TCP）电流，基于此提出了在线监测 IGBT 模块中 FRD 键合线老化状态的方法。该方法无需结温测量，只需在 FRD 正向特性曲线的准 TCP 电流下监测正向压降，即可对 FRD 和整个 IGBT 模块的健康状态进行评估。实验测量得到了 IGBT 和 FRD 芯片的输出/正向特性曲线在不同键合线数量下的差异，验证了该方法的有效性，并与 IGBT 芯片的测量结果进行了对比，发现该方法在应用于 FRD 时灵敏度更高。

关键词：在线监测；IGBT 模块；快恢复二极管（FRD）；温度补偿点（TCP）；键合线
中图分类号：TN407　　文献标识码：A　　文章编号：1003-353X（2019）12-0967-09

Online Monitoring Method for Aging of the IGBT Module Based on Quasi-TCP Current of the FRD Chip

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Abstract: In some working conditions such as the converter super-synchronous mode, the fast recovery diode (FRD) in the insulated gate bipolar transistor (IGBT) module is more likely to age than the IGBT. Therefore, online monitoring of the state of the FRD in the IGBT module is critical. The temperature dependence of the forward characteristic curve of the FRD was studied through theory and experiments. The quasi-temperature compensation point (TCP) current was defined. Based on this, a method for online monitoring of the aging state of FRD bonding wires in IGBT modules was proposed. This method needs no measurement of the junction temperature but monitoring the forward voltage under the quasi-TCP current of the FRD forward characteristic curve, and the health status of the FRD and the whole IGBT module can be evaluated. The difference of the output/forward characteristic curves of the IGBT and FRD chip with different number of bonding wires was measured. The effectiveness of the method was verified.

半导体检测与设备
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三维集成电路中硅通孔复合故障的检测与诊断

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摘要：在硅通孔（TSV）制造工艺中，TSV 不可避免会出现电阻开路和电流泄漏同时存在的复合故障，且相比 TSV 单一故障，复合故障会大大降低三维集成电路的可靠性。以 TSV 作为环形振荡器的负载，以环形振荡器的振荡周期与占空比为测试参数，提出了一种基于粒子群优化（PSO）的最小二乘支持向量机（LSSVM）的故障诊断模型。利用不同故障类型的振荡周期与占空比的数据来训练 LSSVM，采用 PSO 优化 LSSVM 的结构参数，提高了模型诊断的效率与正确率。仿真结果表明，该方法不仅能够检测出故障，还可以将故障进行分类，即开路故障、泄漏故障以及不同程度的复合故障。采用 LSSVM 的平均故障诊断正确率为 95.17%，而采用 PSO 优化后的 LSSVM，平均故障诊断正确率达到 97.17%。

关键词：硅通孔（TSV）；TSV 复合故障；集成电路；粒子群优化（PSO）；最小二乘支持向量机（LSSVM）；环形振荡器

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Detection and Diagnosis of TSV Composite Faults in 3D Integrated Circuits

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Abstract: In the manufacturing process of through-silicon via (TSV), TSVs inevitably appear composite faults with both open-circuit and current leakage. Compared with TSV single faults, composite faults greatly reduce the reliability of three-dimensional (3D) integrated circuits. A fault diagnosis model based on the least squares support vector machine (LSSVM) optimized by particle swarm optimization (PSO) was proposed. TSV was used as a load of the ring oscillator, and the oscillation period and duty cycle of the ring oscillator were used as test parameters. LSSVM was trained with data of oscillation periods and duty cycles of different fault types, and the structural parameters of the LSSVM were optimized by PSO, which improved the efficiency and accuracy of the model diagnosis. The simulation results show that the method can detect faults and classify them into open faults, leakage faults and composite faults with different degrees. The average accuracy of fault diagnosis using LSSVM is 95.17%, and the average accuracy of fault diagnosis using LSSVM optimized by PSO is 97.17%.

Key words: through-silicon via (TSV); TSV composite fault; integrated circuit; particle swarm optimization (PSO); least squares support vector machine (LSSVM); ring oscillator

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显微红外测温中功率器件的边缘效应及其修正

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摘要：针对显微红外热成像中对功率器件进行测温时边缘效应引起的测温误差，提出了采用精密位置调节装置进行修正的方法。分析了显微红外测温中边缘效应产生的原因，认为热膨胀等因素造成了被测功率器件表面两种不同发射率的材料与显微红外热像仪相对位置发生改变，并在两种材料的边缘区域导致明显的测温误差。在理论分析的基础上提出了判断被测件与显微红外热像仪相对位置改变方向的方法，并用显微红外热像仪进行了实验验证。根据被测件表面不同材料的发射率以及测温误差的正负可以判断被测件位置改变的方向，采用精密位移装置补偿这一位置改变即可有效消除边缘效应引起的测温误差。

关键词：显微红外热成像；边缘效应；发射率；位移；测温误差；功率器件
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Edge Effect of Power Devices and the Correction in the Infrared Micro-Thermography

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Abstract: Aiming at the temperature measurement errors caused by the edge effect of power devices in infrared micro-thermography, a correction method using a precise position-adjusting implement was proposed. The causes of the edge effect in the infrared micro-thermography were analyzed. It is considered that thermal expansions or other factors caused the relative position change of two kinds of materials with different emissivity on the surface of the measured power device and the infrared microscope, which made apparent errors near the edge region of the two mateials. Based on the theoretical analysis, the way to determine the direction of the relative position change of the device under test (DUT) and the infrared microscope was proposed, and was validated using an infrared microscope. According to the emissivity of different materials on the surface of the DUT and positive or negative values of temperature measurement errors, the position change direction of the DUT was determined. Using a precise position-adjusting implement to compensate the position change can effectively eliminate the temperature measurement errors caused by the edge effect.

Key words: infrared micro-thermography; edge effect; emissivity; displacement; temperature measurement error; power device

EEACC: 8170G