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射频/微波能量收集系统的整流电路研究进展

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摘要：射频/微波能量收集系统以可持续、环保等优点在无线传感器网络、可穿戴设备等领域具有广泛应用前景。对近年来射频/微波能量收集系统的整流电路的研究进展进行了概述。分析并讨论了整流电路的技术指标和电路结构，分别从器件研究和电路设计两个方面对整流电路的研究进展进行分析、归纳。从原理、性能提升等方面分析具有低的零偏压电阻值的自旋二极管应用于微瓦量级信号整流电路的潜力；从微弱信号整流、宽输入功率范围信号整流、高功率转换效率整流、阻抗去敏感化4个方面分析了整流电路设计的关键问题，归纳出有效的解决途径并对整流电路的发展趋势进行了展望。

关键词：射频/微波能量收集系统；整流电路；自旋二极管；宽输入功率范围；阻抗去敏感化

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Research Progress of the Rectifier for the RF/Microwave Energy Harvesting System

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Abstract: The RF/microwave energy harvesting system has broad application prospects in the fields of wireless sensor networks and wearable devices due to the advantages of sustainable development and environmental protection. The research progress of the rectifier for the RF/microwave energy harvesting system in recent years is reviewed. The technical specifications and circuit structure of the rectifier are analyzed and discussed. The research progress of the rectifier is analyzed and summarized from two aspects of device research and circuit design. The application potential of the spin diode with low zero bias resistance in microwatt level power rectifier is analyzed from the operating principle, performance enhancement and so on. Key issues of the rectifier design are analyzed from four aspects: weak signal rectification, operating in wide input power range, high power conversion efficiency rectification and mitigating resistance sensitivity. Effective solutions are summarized and the development trend of rectifier is prospected.

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一种应用于 CAN 总线芯片的过压保护电路设计

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摘要：为解决传统过压保护电路功耗大、易受干扰的问题，基于 0.25 μm CMOS 工艺设计并实现了一种应用于控制器局域网络（CAN）总线芯片的过压保护电路。其作用是当芯片端口电压高于电源电压或低于地（GND）电平时为芯片提供保护信号，阻止电流倒灌入芯片。在 3.3 V 电源电压下，该电路具有迟滞功能，防止其受到噪声干扰反复打开和关闭芯片。仿真结果表明，端口电压高于 3.55 V 时电路提供保护信号，重新下降至 3.35 V 后系统恢复工作；同理，端口电压低于-0.25 V 时电路提供保护信号，重新上升至-0.05 V 后系统恢复工作。流片测试结果显示该电路可以为 CAN 总线芯片提供有迟滞的过压保护功能，与符合仿真结果基本一致。

关键词：控制器局域网络（CAN）总线；CMOS；过压保护；迟滞；低功耗

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Design of an Overvoltage Protection Circuit Applied to the CAN Bus Chip

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Abstract: An overvoltage protection circuit applied to the controller area network (CAN) bus chip was designed and implemented based on the 0.25 μm CMOS process to solve the problem of high power consumption and sensitive to the interference of traditional overvoltage protection circuits. As the port voltage of the chip is higher than power supply voltage or lower than GND voltage, the circuit can provide a protective signal for the chip to prevent the current flow backward into the chip. At a power supply voltage of 3.3 V, the circuit has a hysteresis function to prevent it from turning on and off repeatedly caused by the noise interference. The simulation results show that the circuit provides a protection signal for the chip when the port voltage is higher than 3.55 V and restarts to work when the port voltage is lower than 3.35 V. Similarly, the circuit provides a protection signal for the chip when the port voltage is lower than −0.25 V and restarts to work when the port voltage increases to −0.05 V. The test results show that the circuit can provide the function of overvoltage protection and hysteresis for CAN bus chip, which is basically consistent with the simulation results.

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新型基区结构高反压功率晶体管的优化

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摘要：依据电参数指标要求，针对高压-高增益硅功率晶体管基区结构和终端结构进行优化研究。提出了一种可用于改善集电极-发射极击穿电压（$V_{(BR)CEO}$）和电流放大倍数（β）矛盾关系的带埋层的新型基区结构，并针对埋层基区结构对高压-高增益硅功率晶体管电性能及可靠性的影响进行了研究。仿真结果表明：新型基区结构不仅可以很好地折中晶体管β与$V_{(BR)CEO}$之间的矛盾关系，而且还能在较大的埋层基区宽度、埋层基区掺杂峰值浓度范围内使晶体管获得较低且一致性较好的饱和压降；具有新型基区结构的晶体管在改善正偏的情况下抗二次击穿能力具有明显优势。由仿真得到的器件结构参数，研制出的样片的β，$V_{(BR)CEO}$和集电极-基极击穿电压（$V_{(BR)CBO}$）均满足电参数指标要求。

关键词：高增益；功率晶体管；埋层基区；终端保护；击穿电压
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Optimization of the High Reverse Voltage Power Transistor with New Type Base Structure

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Abstract: According to the electrical parameter requirements, the optimization of the base structure and terminal structure of high-voltage and high-gain silicon power transistor was studied. A new base structure with buried layer which can improve the contradiction between the collector-emitter breakdown voltage ($V_{(BR)CEO}$) and the current amplification (β) was proposed. In addition, the influences of the buried layer structure on the electrical performance and reliability of high-voltage and high-gain silicon power transistors were studied. The simulation results show that the new base structure can compromise the contradiction between β and $V_{(BR)CEO}$, and achieve a low and consistent saturation voltage drop within a larger range of width and the peak doping concentration of the buried base region. The transistor with new base structure has an obvious advantage in resisting the secondary breakdown under the condition of improving positive bias. According to the device structure parameters obtained by simulation, β, $V_{(BR)CEO}$ and collector base breakdown voltage ($V_{(BR)CBO}$) of the sample meet the requirements of the electrical parameters.

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一种新型隧穿场效应晶体管

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摘要：提出了一种新型隧穿场效应晶体管（TFET）结构，该结构通过在常规 TFET 靠近器件栅氧化层一侧的漏-体结界面引入一薄层二氧化硅（隔离区），从而减小甚至阻断反向栅压情况下漏端到体端的带带隧穿（BTBT），减弱 TFET 的双极效应，实现大幅度降低器件泄漏电流的目的。利用 TCAD 仿真工具对基于部分耗尽绝缘体上硅（PDSOI）和全耗尽绝缘体上硅（FDSOI）的 TFET 和新型 TFET 结构进行了仿真与对比。仿真结果表明，当隔离区宽度为 2 nm，高度大于 10 nm 时，可阻断 PDSOI TFET 的 BTBT，其泄漏电流下降了 4 个数量级；而基于 FDSOI 的 TFET 无法彻底消除 BTBT 和双极效应，其泄漏电流下降了 2 个数量级。因此新型结构更适合于 PDSOI TFET。

关键词：隧穿场效应晶体管（TFET）；绝缘体上硅（SOI）；泄漏电流；带带隧穿（BTBT）；双极效应

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A New Type of Tunneling-FET

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Abstract: A new structure of tunneling-FET (TFET) was proposed. A thin layer of SiO_2 was inserted into the interface of the junction of drain and bulk near the gate-oxide side of the traditional TFET to eliminate or even to block band to band tunneling (BTBT) under a reverse gate bias condition, the bipolar effect of the TFET was decreased, and the leakage current was reduced greatly. The structures of the traditional TFET and the new TFET based on partially depleted silicon-on-insulator (PDSOI) and fully depleted silicon-on-insulator (FDSOI) were simulated and compared with TCAD simulation tools. The simulation results show that the BTBT of the PDSOI TFET can be blocked when the isolation region is 2 nm wide and the height is greater than 10 nm, and the leakage current is reduced by 4 orders of magnitude; the BTBT and bipolar effects of the FDSOI TFET cannot be eliminated completely, and the leakage current is reduced by 2 orders of magnitude. Therefore, the new structure is more suitable for the PDSOI TFET.

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Cu/SiO_2 逐层沉积增强无杂质空位诱导 InGaAsP/InGaAsP 量子阱混杂

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摘要：研究了 Cu/SiO_2 逐层沉积增强的无杂质空位诱导 InGaAsP/InGaAsP 多量子阱混杂（QWI）行为。在多量子阱（MQW）外延片表面，采用等离子体增强的化学气相沉积（PECVD）不同厚度的 SiO_2，然后溅射 5 nm Cu，在不同温度下进行快速热退火（RTA）诱发量子阱混杂。通过光荧光（PL）谱表征样品在 QWI 前后的变化。实验结果表明，当 RTA 温度小于 700 ℃时，PL 谱峰值波长只有微移，且变化与其他参数关系不大；当 RTA 温度大于 700 ℃时，PL 谱峰值波长移动与介质层厚度和 RTA 时间都密切相关，当 SiO_2 厚度为 200 nm，退火温度为 750 ℃，时间为 200 s 时，可获得 54.3 nm 的最大波长蓝移。该种 QWI 方法能够诱导 InGaAsP MQW 带隙移动，QWI 效果与 InGaAsP MQW 中原子互扩散激活能、互扩散原子密度以及在 RTA 过程中热应力有关。

关键词：InGaAsP；多量子阱（MQW）；量子阱混杂（QWI）；Cu/SiO_2；快速热退火；蓝移

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InGaAsP/InGaAsP Quantum Well Intermixing Induced by Impurity Free Vacancy Enhanced Through Cu/SiO_2 Deposition

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Abstract: InGaAsP/InGaAsP multiple quantum well intermixing (QWI) behavior induced by impurity free vacancy enhanced through Cu/SiO_2 deposition was investigated. On the surface of the multiple quantum well (MQW) epitaxial wafer, different thickness of SiO_2 were grown by plasma-enhanced chemical vapor deposition (PECVD), then 5 nm of Cu was sputtered, after rapid thermal annealing (RTA) at different temperatures, QWI was induced. Changes of the samples before and after QWI process were characterized by photoluminescence (PL) spectra. The experimental results show that the peak wavelength of the PL spectrum shifts slightly when the RTA temperature is less than 700 ℃, and the change has little relationship with other parameters. When the RTA temperature is greater than 700 ℃, the peak wavelength shift of the PL spectrum is closely related to the thickness of dielectric layer and RTA time. When the SiO_2 thickness is 200 nm, and the wafer is annealing at 750 ℃ for 200 s, the maximum wavelength blue shift is 54.3 nm. The QWI method can induce the band gap shift of InGaAsP MQW. The QWI effect is related to atomic interdiffusion activation energy, interdiffusion atom density and

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40 nm 节点高深宽比接触孔刻蚀电性能稳定性改善

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摘要：随着工艺节点减小，对高深宽比接触孔形貌和关键尺寸的精准控制变得愈加困难。基于 40 nm 逻辑器件量产数据，研究了高深宽比接触孔刻蚀工艺参数和刻蚀设备内部耗材的磨损对器件电性能稳定性的影响，并提出了工艺改进方案。通过减小 SiO_2 厚度，减小接触孔深宽比，从而改善孔内聚合物在孔底部沉积的问题；通过优化刻蚀工艺参数提高 SiN/SiO_2 刻蚀选择比，保持刻蚀后 SiO_2 的厚度与改进前工艺相同。测试结果表明，工艺改进后接触孔底部关键尺寸稳定性提升 36%，接触电阻稳定性提升 20%。通过工艺改进提高了电参数稳定性，对 40 nm 工艺节点逻辑器件产品良率提升起到了关键作用。

关键词：高深宽比；接触孔刻蚀；侧壁形貌；刻蚀选择比；接触电阻；刻蚀设备耗材

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Electric Stability Improvement of High Aspect Ratio Contact Hole Etching in 40 nm Process Node

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Abstract: As the process nodes decrease, it becomes more difficult to control the morphology and critical dimensions of the high aspect ratio contact hole accurately. Based on the mass production data of the 40 nm logic devices, the influences of etching process parameters of high aspect ratio contact holes and the consumable parts of the etching equipment on the stability of the device electrical parameters were studied and a process improvement scheme was proposed., The polymer residue in the bottom of the holes was improved by reducing the thickness of SiO_2 and the aspect ratio of the contact holes. The thickness of SiO_2 after etching was the same as the original process by optimizing process parameters to improve the selection ratio of SiN/SiO_2 etching. The test results show that the stability of the critical dimension of the bottom of the contact holes increases by 36% and the stability of the contact resistance increases by 20%. The stability of the electrical parameters is improved by improving the existing process, which plays a key role in improving the yield of 40 nm process node logic devices.

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半导体激光密集谱合束中 VBG 的热效应

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摘要：研究并分析了半导体激光密集谱合束技术中体布拉格光栅（VBG）的热效应问题。为了提高半导体激光器的输出功率及其电光转换效率，利用 COMSOL 软件模拟了半导体激光器中 VBG 在自由传导散热和水循环冷却两种条件下的温度分布，通过对比这两种条件下 VBG 温度对其中心波长漂移量及输出功率的影响，分析了 VBG 热效应变化。模拟与实验结果表明，水循环冷却可以有效将 VBG 的温度从 390.44 K 降低到 299.09 K，减小了 VBG 的波长漂移量，有效抑制了 VBG 的热效应问题。因此合理控制 VBG 的温度，可提高半导体激光器的输出功率和电光转换效率。

关键词：半导体激光；体布拉格光栅（VBG）；水循环冷却；热效应；电光转换

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Thermal Effect of VBG in Semiconductor Laser Dense Spectrum Synthesis

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Abstract: The thermal effect of the volume Bragg grating (VBG) in semiconductor laser dense spectrum combining technology was studied and analyzed. In order to improve the output power and electro-optic conversion efficiency of the semiconductor laser, the temperature distributions of VBG in the semiconductor laser under free conduction cooling and water cycle cooling were simulated by COMSOL software. The variation of VBG thermal effect was analyzed by comparing the effects of VBG temperature on the central wavelength drift and output power under the two conditions. The simulation and experiment results show that the temperature of the VBG is reduced from 390.44 K to 299.09 K effectively under water cycle cooling, the wavelength drift of VBG is reduced, and the VBG thermal effect is suppressed effectively. Therefore reasonably controling the temperature of the VBG can improve the output power and the electro-optic conversion efficiency of the semiconductor laser.

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层压封装平面 LED 光源的耐候实验

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摘要：研究了层压封装的平面 LED 光源在高温高湿与水下环境的可靠性。平面 LED 光源采用标准层压工艺封装，对封装后的 LED 模组进行高温高湿耐候试验与水下环境试验，并与未封装的 LED 模组进行对比实验。实验结果表明，在环境温度为 80 ℃、相对湿度为 80%，模组工作电流为 300 mA，连续 33 天高温高湿条件下，层压封装的平面 LED 模组的照度变化和温度均高于未封装的 LED 模组。在 40 ℃水下环境下连续工作 400 h，层压封装的平面 LED 模组的照度略有变化，且光衰小于 1%。因此，层压封装能有效阻断外界高温高湿环境对 LED 模组可靠性的影响，更适合在常温水下照明应用。

关键词：平面 LED 光源；层压封装；耐候实验；可靠性；水下环境实验
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Weathering Test of Laminated Package Plane LED Light Source

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Abstract：The reliability of the plane LED light source with laminated package was studied in high temperature，high humidity and underwater environment. The plane LED light source was packaged by a standard laminated packaging process. High temperature and high humidity weathering test and underwater environment experiment were carried out on the encapsulated and unencapsulated LED modules，respectively. The test results show that compared with the unpackaged LED modules，the variation of illuminance of the laminated plane LED modules are larger and the temperature are higher after working at ambient temperature of 80 ℃ and relative humidity of 80% under a current of 330 mA for 33 days continuously. After continuous operation for 400 h in 40 ℃ underwater environment，the illuminance of the laminated plane LED modules change slightly，and the light decay is less than 1%. Therefore，the laminated package can effectively block the influences of the high temperature and high humidity environment on the reliability of the LED modules，and is more suitable for the underwater lighting application at room temperature.

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一种陶瓷方形扁平封装外观缺陷检测方法

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摘要：提出一种基于机器视觉的陶瓷方形扁平封装外观缺陷检测方法。对于封装外形尺寸较大而缺陷较细微的情形，将待检片分为多个区域与标准样片进行比对检测。首先通过 Foerstner 特征点检测法提取标准片图像的特征点，然后使用随机抽样一致性（RANSAC）图像匹配算法，将所有标准片图像拼接并融合生成一张标准片全幅面模板，再将待检片分区与标准片模板进行序贯比对，以提取可疑区域，最后利用支持向量机（SVM）分类器对可疑区域进行筛选分类。实验结果表明，这种方法不仅克服了传统视觉检测过程中视野范围与图像分辨率相互制约的矛盾，且对陶瓷方形扁平封装表面缺陷具有较高的检出率。

关键词：缺陷检测；陶瓷方形扁平封装；图像拼接；样本提取；支持向量机（SVM）分类器

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A Defects Detection Method for Ceramic Quad Flat Package Appearance

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Abstract: A machine-vision-based defect detection method for ceramic quad flat package appearance was proposed. For case of larger package size and smaller defects, the sample to be inspected was divided into several regions and compared with the standard sample. Firstly, the feature points of the standard image were extracted by Foerstner feature point detection method. Then all the standard images were stitched and merged by random sample consensus (RANSAC) image matching algorithm to generate a standard full-frame template. And then the sample to be inspected was compared with the standard template sequentially to extract the suspicious area. Finally the suspicious region was filtered and classified by using the support vector machine (SVM) classifier. The test results show that the proposed method can overcome the contradiction between the visual field range and the image resolution in the traditional visual inspection process, and has a high detection rate for the ceramic quad flat package surface defects.

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一款消除浮空点并自锁存的老化预测传感器

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摘要：针对负偏置温度不稳定性引起的组合逻辑电路老化，提出了一款消除浮空点并自锁存的老化预测传感器。该传感器不仅可以预测组合逻辑电路老化，而且能够通过传感器内部的反馈来锁存检测结果，同时解决稳定性校验器在锁存期间的浮空点问题，其延时单元为可控型延时单元，可以控制其工作状态。使用 HSPICE 软件进行仿真，验证了老化预测传感器的可行性，可以适用于多种环境中且不会影响传感器性能。与同类型结构相比，该传感器的稳定性校验器能够对检测结果进行自锁存，使用的晶体管数量减少了约 8%，平均功耗降低了约 20%。

关键词：传感器；老化预测；自锁存；浮空点；逻辑电路；负偏置温度不稳定性

中图分类号：TP212　　**文献标识码**：A　　**文章编号**：1003-353X（2019）03-0216-07

A Floating Point Eliminated and Self-Latching Aging Prediction Sensor

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Abstract: Aiming at the aging of combinational logic circuits caused by negative bias temperature instability, a floating point eliminated and self-latching aging prediction sensor was proposed. The sensor can predict the aging of the combinational logic circuit, and can latch the detection result through the feedback inside the sensor. Meanwhile, it can solve the floating point problem of the stability checker during latching. Delay unit of the sensor is controllable delay unit, which can control its working state. HSPICE simulation results show that the sensor is feasible and can be used in many environments without affecting the performance of the sensor. Compared with the same type of structure, the stability checker of the sensor can latch up the predicted results, the number of transistors used in the sensor is reduced by about 8%, and average power consumption is reduced by about 20%.

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90 kW/3 000 A 高压大功率 IGBT 器件功率循环测试装备研制

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摘要：随着高压大功率 IGBT 器件容量的进一步提升，对考核其可靠性的功率循环测试装备在测量精度、测试效率和长期运行可靠性等方面提出了挑战。针对柔性直流输电系统用高压大功率 IGBT 器件的测试需求，基于现有功率循环测试方法，增加了测试支路和辅助支路，提高了测试装备的测量精度和测试效率，增强了装备的长期运行可靠性，搭建了 90 kW/3 000 A 功率循环测试装备。针对应用于柔性直流输电的两种不同封装形式高压大功率 IGBT 器件——压接型 IGBT 器件和焊接式 IGBT 模块分别设计了相应的测试夹具，满足了柔性直流输电工程的需求，并基于此装备对不同封装形式和电流等级的器件进行了 400 多万次的功率循环测试，验证了测试装备的测试功能和长期运行可靠性。

关键词：柔性直流输电系统；压接型 IGBT 器件；焊接式 IGBT 模块；长期运行可靠性；功率循环测试

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Development of 90 kW/3 000 A Power Cycling Test Equipment for High Voltage and High Power IGBT Modules

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Abstract: Power cycling test equipment with higher accuracy, efficiency and long life-time reliability is strongly needed to meet the requirements of high power IGBTs with higher power density. A 90 kW/3 000 A power cycling test equipment was built according to the requirements of high power IGBTs applied in the flexible HVDC transmission system. Based on the basic test circuit of the power cycling test, two test branches and one auxiliary branch were added to improve the test accuracy, efficiency and long life-time reliability of the test equipment. the corresponding test fixtures were respectively designed for press pack IGBTs and power IGBT modules which were two different packaging styles of high-voltage and high-power IGBT devices to meet the requirements of the flexible HVDC transmission system. More than 4 000 000 cycles in total have been conducted for different packaging styles and current ratings up to now by this equipment. The basic test functions and long life-time reliability of this power cycling test equipment are verified by these cycles.

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片上皮法级电容测试系统专用标准件的研制

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摘要：研制了一套用于片上皮法级电容测试系统的电容标准件，量值低至 1 pF，频率达到 1 MHz。该电容标准件采用 GaAs 衬底，金属-绝缘层-金属（MIM）结构的电容器阵列实现，其标称值分别为 1，10 和 100 pF。为了消除由探针系统和外界环境引入的分布电容的影响，在芯片同一单元内设计了在片开路器，电容测量准确度达到±1%。建立了在片皮法级电容测量模型，利用组建的可溯源在片定标装置对电容样片定标后，进行重复性和稳定性考核，最终研制出年稳定性小于 0.4%的电容标准件一套。测量结果及标准件应用表明，研制的标准件可为片上皮法级电容测试系统进行现场整体校准。

关键词：片上皮法级电容测试系统；在片开路器；MIM 电容；测量模型；在片电容标准件
中图分类号：TN304.23；TB971　**文献标识码**：A　**文章编号**：1003-353X（2019）03-0232-07

Development of Capacitance Standards for On-Chip pF-Capacitance Test System

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Abstract: A set of capacitance standards which has a nominal capacitance value as low as 1 pF and the operating frequency up to 1 MHz were developed for on-chip pF-capacitance test system was realized using an array of the metal-insulator-metal (MIM) capacitors on GaAs substrate, and the nominal values are 1, 10 and 100 pF, respectively. In order to compensate the influences of the stray capacitance introduced by the probe system and outer environment, an on-chip open was designed in the same cell on the chip, and the accuracy of the capacitance measurement reached to ±1%. An on-chip pF-capacitance measurement model was built, and the capacitance samples were calibrated by using the established on-chip calibration equipment. After assessing the repeatability and stability, a set of capacitance standards were finally produced with the annual stability of 0.4%. Measurement results and standards application shows that the standards can be used for the overall on-site calibration by the on-chip pF-capacitance test system.